IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A method of forming a non-gated silicon on insulator diode in a semiconductor substrate, the substrate including a plurality of isolation regions formed therein, said method comprising:

forming a first structure on an upper surface of said substrate in a region between at least one pair of said isolation regions;

forming a first region of a first dopant type in said substrate, said first region comprising a first edge aligned to a first edge of said first structure; ~~and~~

forming a second region of a second dopant type in said substrate, said second region comprising a second edge aligned to a second edge of said first structure, said second region being of a different dopant type than said first region;

removing said first structure.

2. (Currently Amended) The method of claim 1, further comprising: ~~forming a second region of a second dopant type in said substrate, the second region comprising a second edge aligned to a second edge of said first structure~~

forming said first region and said second region in said area between said least one pair of isolation regions in said substrate and below said first structure;

forming a diode junction in between said first region and said second region; and

aligning an upper surface of said diode junction with said first structure.

3. (Original) The method of claim 1, further comprising forming a first silicide layer comprising a first silicide edge aligned to said first edge of said first structure.

4. (Currently Amended) The method of claim [[2]] 1, further comprising forming a second silicide layer comprising a second silicide edge aligned to said second edge of said first structure.

5. (Original) The method of claim 1, wherein said first structure comprises a hard mask.

6. (Original) The method of claim 5, wherein said hard mask comprises a silicon nitride layer.

7. (Original) The method of claim 1, wherein said first structure comprises a gate.

8. (Original) The method of claim 7, wherein said first structure further comprises insulating spacers.

9. (Original) The method of claim 8, wherein in said removing step, said spacers remain on said substrate.

10. (Currently Amended) A method of forming a self-aligned SOI diode, said method

comprising:

depositing a protective structure over a substrate, wherein said protective structure comprises a polysilicon gate;

implanting a plurality of diffusion regions of variable dopant types in an area between at least one pair of isolation regions in said substrate, said plurality of diffusion regions separated by a diode junction, wherein said implanting aligns an upper surface of said diode junction with said protective structure; and

removing said protective structure.

11. (Original) The method of claim 10, further comprising forming a silicide layer over said diffusion regions and aligned with said protective structure.

12. (Original) The method of claim 10, wherein said protective structure comprises a hard mask.

13. (Original) The method of claim 12, wherein said hard mask comprises a silicon nitride layer.

14. (Currently Amended) The method of claim 10, wherein said ~~protective structure comprises a polysilicon gate~~ plurality of diffusion regions of variable dopant types comprise:

a first region comprising a first dopant type; and

a second region comprising a second dopant type.

wherein said first dopant type is a different dopant type than said second dopant type.

15. (Currently Amended) The method of claim [[14]] 10, wherein said protective structure further comprises insulating spacers.

16. (Original) The method of claim 15, wherein in said removing step, said spacers remain on said substrate.

17. (Original) A method of forming a self-aligned silicon over insulator diode, said method comprising:

implanting an N-well doping region in an implant region in between isolation regions in a semiconductor substrate;

configuring a gate over said implant region;

configuring a pair of sidewall spacers on sides of said gate;

using said gate to define P+ and N+ contact regions in said implant region;

removing said gate; and

using said sidewall spacers to align a silicide layer over said P+ and N+ contact regions.

18. (Original) The method of claim 17, further comprising defining a diode junction region in between the P+ and N- regions and the N+ and N- regions.

19. (Original) The method of claim 17, further comprising removing said sidewall spacers.

20. (Original) The method of claim 17, further comprising depositing said silicide layer over said N-well doping region.